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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,184	10/31/2003	John T. Gasner	125.090US01	2505

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EXAMINER	
LEE, HSIEN MING	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/698,184	GASNER ET AL.	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *39-63,66,67 and 85-98* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *39-42, 44, 46, 48-51, 53, 56, 57, 60, 61, 63, 66, 67, 90- 92 and 94* is/are rejected.

7)☒ Claim(s) *43,45,47,52,54,55,58,59,62,85-89,93 and 95-98* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

HSIEN-MING LEE
PRIMARY EXAMINER

11/2/04

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *111204*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. Applicant's election to claims 39-63, 66-67 and 85-98 and cancellation to claims 1-38, 65-65 and 68-84 is acknowledged.

Claim Objections

2. Claims 39, 41, 47, 57, 58, 60, 63, 85, 87-89, 92-93 and 95-98 are objected to because of the following informalities:

In claim 39 (line 6), changing "the first insulating layer" into – the first layer of relatively thick insulating material -- is suggested.

In claim 39 (line 9), changing " the top layer" into – the top metal layer – is suggested.

In claim 41 (line 2), claim 63 (lines 2 and 4), claim 85 (lines 3 and 4), claim 87 (lines 2 and 4), claim 88 (lines 2-3), claim 89 (line 1), claim 92 (lines 2 and 4), claim 93 (line 5), claim 95 (lines 5, 7, 9, 10, 12 and 13), claim 96 (line 1), claim 97 (lines 3, 7 and 8), and claim 98 (lines 2, and 4), changing " one or more" into – at least one – or – a plurality of – is suggested.

In claim 47, inserting – is – before "TiN" is needed.

In claim 57, at line 4, changing "first metal region" into – first metal layer – is needed.

In claims 58 and 60, changing "relatively thick" into – relatively stiff – is needed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 39, 50, 67, 90, 92 and 94 are rejected under 35 U.S.C. 102(b) as being anticipated by Henson (US 6,133,054).

In re claim 39, Henson, in Fig.7 and related text, teaches the claimed method of forming an integrated circuit with circuitry under a bond pad, the method comprising:

- forming devices 704 in and on a substrate 706;
- forming a first metal layer 712;
- forming a first layer of relatively thick insulating material 716 overlaying the first metal layer 712, wherein the thickness of the first insulating layer 716 strengthens the integrated circuit;
- forming a top metal layer 718 overlaying the relatively thick insulating layer 716 (Fig.4); and
- forming a bond pad 112 on a surface of the top metal layer 718.

In re claim 50, Henson teaches the claimed method of forming an integrated circuit, the method comprising:

- forming device regions 704 in a substrate 710/706;
- depositing a first metal layer 712 overlaying the device regions 704;
- pattering the first metal layer 712 to form gaps, wherein the gaps extend in a current flow direction;
- forming an insulating layer 716 overlaying the first metal layer 712 and filling in the gaps, wherein the gaps strengthen the integrated circuit by providing pillars of harder insulating material;
- depositing a top layer of metal 718 overlaying the insulating layer 716; and

- forming a bond pad 112 on a surface of the top layer of metal 718.

In re claim 67, Henson teaches that the bond pad 112 is formed directly over at least one of the device region 704 (Fig.7).

In re claim 90, Henson also teaches the claimed method of forming an integrated circuit, the method comprising:

- forming device regions 704 on and in a substrate 706/710;
- forming a first metal layer 712 overlaying the substrate 706/710;
- forming a top metal layer 718 overlaying the first metal layer 712;
- forming at least one bonding pad 112 on the top metal layer 718; and
- forming a first layer of insulating material 716 separating the top metal layer 718 from the first metal layer 712, wherein the first layer of insulating material 716 has a thickness selected to resist cracking.

In re claim 92, Henson further teaches forming plural intermediate metal layers between the first metal layer 712 and the substrate 706/710; and forming plural insulation layers to separate the plural intermediate metal layers form each other (col. 4, lines 10-13).

In re claim 94, Henson also teaches forming gaps in the first metal layer 712 to form pillars of relatively stiff insulating material 716 passing through the first metal layer 712 (Fig.7).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 39, 41, 42, 44, 46, 48-50, 53, 56, 57, 60, 63 and 66 are rejected under 35 U.S.C. 102(e) as being anticipated by Imai et al. (US 2003/0045088).

In re claim 39, Cook et al., in Figs.3 ~11 and related text, teach the claimed method of forming an integrated circuit with circuitry under a bond pad, the method comprising:

- forming devices MISFET 5/6/7 in and on a substrate 1;
- forming a first metal layer 11 (Fig.3);
- forming a first layer of relatively thick insulating material 12/15 overlaying the first metal layer 11 (Fig.3), wherein the thickness of the first insulating layer 12/15 strengthens the integrated circuit;
- forming a top metal layer 18A/18B overlaying the relatively thick insulating layer 12/15 (Fig.4); and
- forming a bond pad 21B/22B and 23D on a surface of the top metal layer 18A/18B (Figs.10-11).

In re claim 41, Cook et al teach forming one intermediate metal layer 10/11 between the devices MISFET 5/6/7 and the first metal layer 11 (Fig.3).

In re claim 42, Cook et al teach patterning the first metal layer 11 to form gaps (Fig.3).

In re claim 44, Cook et al. teach that the gaps are formed to be oriented such that the impact on the current flow through the first metal layer 11 is minimized.

In re claims 46 and 48, Cook et al. also teach forming a sub-layer of relatively stiff material 19 (Fig.10), wherein the stiff material 19 can be silicon nitride (paragraph [0096]).

In re claims 49, Cook et al. teach that the relatively stiff material 19 is formed near the first layer of relatively thick insulating material 12/15 (Fig.10).

In re claim 50, Cook et al. teach the claimed method of forming an integrated circuit, the method comprising:

- forming device regions MISFET 5/6/7/ in a substrate 1/4/9;
- depositing a first metal layer 11 overlaying the device regions MISFET 5/6/7;
- pattering the first metal layer 11 to form gaps, wherein the gaps extend in a current flow direction;
- forming an insulating layer 12/15 overlaying the first metal layer 11 and filling in the gaps, wherein the gaps strengthen the integrated circuit by providing pillars of harder insulating material;
- depositing a top layer of metal 18A/18B overlaying the insulating layer 12/15; and
- forming a bond pad 21B/22B and 23D on a surface of the top layer of metal 18A/18B.

In re claims 53 and 56, Cook et al. also teach forming a sub-layer of relatively stiff material 19 adjacent to the insulating layer 12/15 (Fig.10), wherein the stiff material 19 can be silicon nitride (paragraph [0096]).

In re claims 57 and 60, Cook et al., in Figs.3 ~11 and related text, teach the claimed method of forming an integrated circuit with circuitry under a bond pad, the method comprising:

- forming devices regions MISFET 5/6/7 in and on a substrate 1;
- forming a first metal layer 11 overlying the device regions 5/6/7 (Fig.3);
- forming an insulating layer 12/15 overlaying the first metal layer 11 (Fig.3);

- forming a top metal layer 18A/18B overlaying the insulating layer 12/15 including a sub-layer of relatively stiff material 19 near the insulating layer 12/15 (Fig.4), wherein the stiff material 19 can be silicon nitride (paragraph [0096]); and
- forming a bond pad 21B/22B and 23D on a surface of the top metal layer 18A/18B (Figs.10-11).

In re claim 63, Cook et al. also teach forming one intermediate metal layer 14 between the first metal layer 11 and the device regions 5/6/7, and patterning the one intermediate metal layer 14 to form interconnects between the devices (FIG.3).

In re claim 66, Cook et al. teach forming at least one of the devices MISFET 5/6/7 under the bond pad 21B/22B and 23D (Fig.10).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 40, 51, 61 and 91 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imai et al..

In re claims 40, 51, 61 and 91, the selection of the first layer of relatively thick insulating material is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known

process is obvious). In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range. See M.P.E.P. 2144.05, III

Allowable Subject Matter

9. Claims 43, 45, 47, 52, 54-55, 58, 59 and 62 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claim 85 and 95 would be allowable if rewritten or amended to overcome the objection as set forth in this Office action.

11. Claims 86-89 and 96-98 are objected to as being dependent upon an objected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. Claim 93 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record neither teaches nor suggests the gaps take up *no more than 10%* of the total area of the first metal layer under the bond pad (claims 43, 52, 62); the relatively stiff material is *TiN* (claims 47, 54, 58) or is *TiW* (claims 55, 59); at least one sub-layer of material that is relatively *stiff* is adapted to *prevent the cracking* of the one intermediate conductive layer (claim 85); and forming gaps in one of the one intermediate conductive layer closest the top conductive layer, the gaps being adapted to *prevent cracking* of the one intermediate conductive

layers by forming pillars of relatively stiff insulation material passing through the one of the one intermediate conductive layers closest the top conductive layer (claim 95).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on Tuesday-Thursday (8:00 ~ 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-Ming Lee
Primary Examiner
Art Unit 2823

Nov. 12, 2004

HSIEN-MING LEE
PRIMARY EXAMINER

11/12/2004